CHAPTER ONE

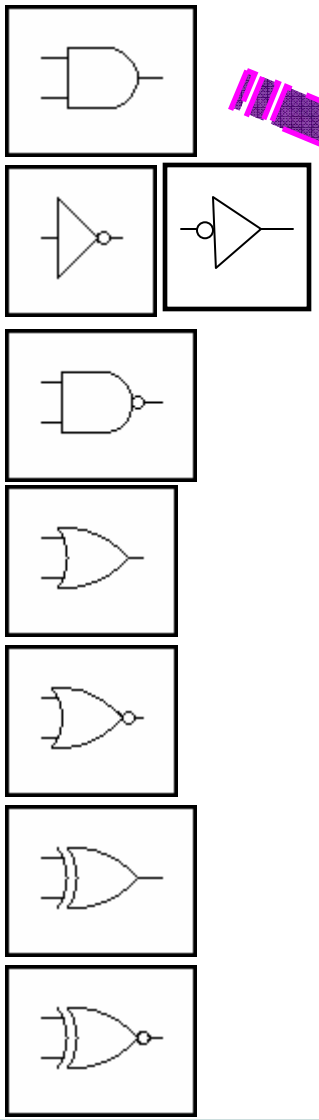
Properties of Digital Integrated Ccts.

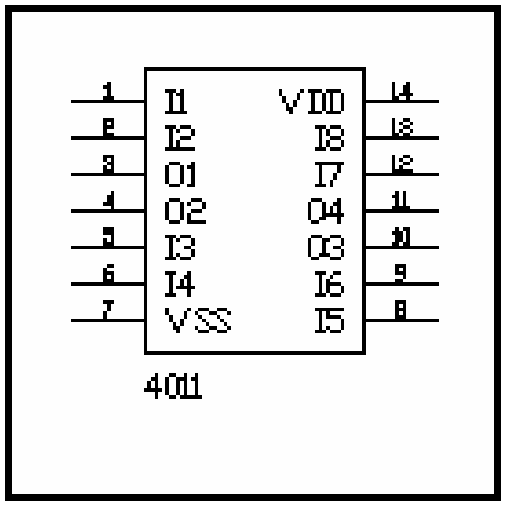
Digital Electronics.

Basic Logic Operations

Ch 1

- AND
- NOT
- NAND
- OR
- NOR
- XOR
- XNOR





4 2-in AND

4 inputs with two AND gates

Basic Logic Operations

- Combinantional logic:

  Output depends only on present value of the input.

- Sequential logic:

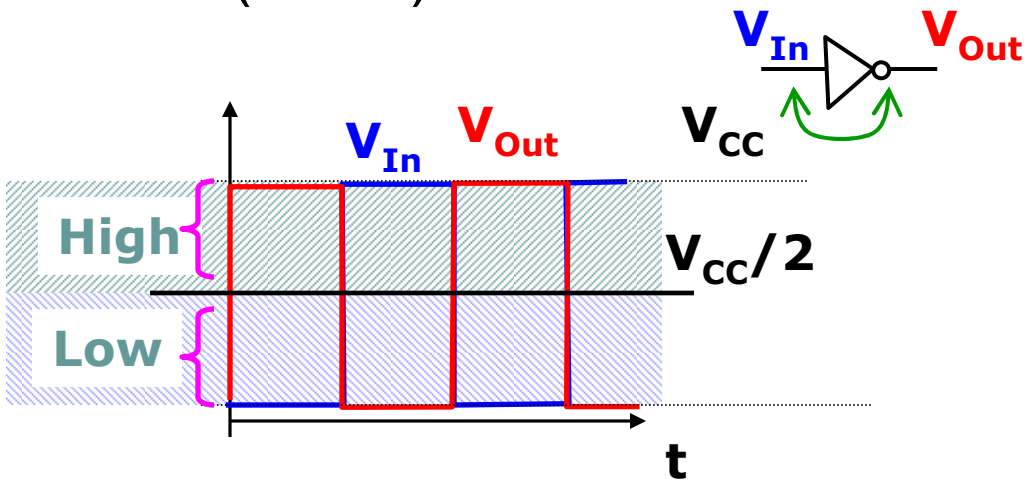
  Output depends on present/past value of the input.

Basic Logic Operations

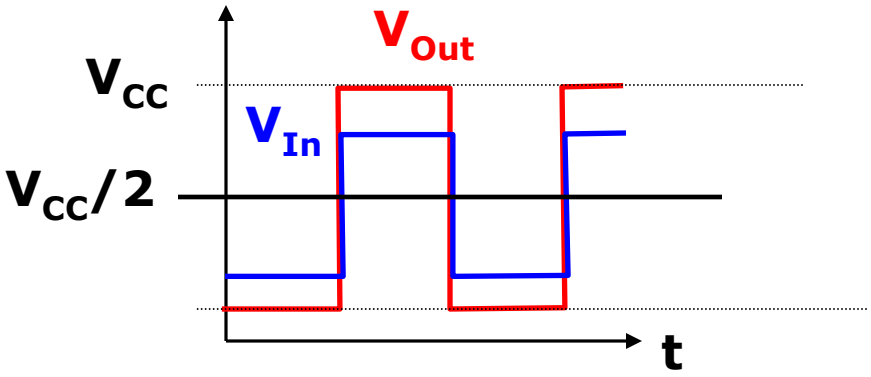
- The voltages/currents in digital logic circuits have two possible states (*according to positive voltage logic*)√:
  - Low voltage corresponds to a binary 0
  - High voltage corresponds to a binary 1
- *But according to negative voltage logic:*
  - *Low voltage corresponds to a binary 1*
  - *High voltage corresponds to a binary 0*

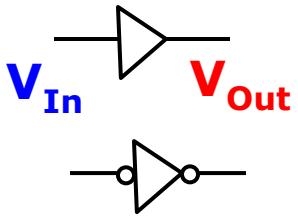
Basic Building Blocks

- Inverter (NOT)



- Non-inverter (Buffer)

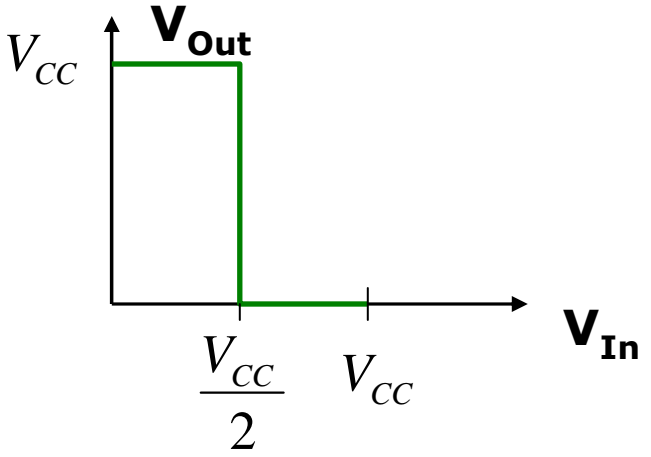




Used to regenerate voltage levels by making degraded high levels higher and degraded low levels lower

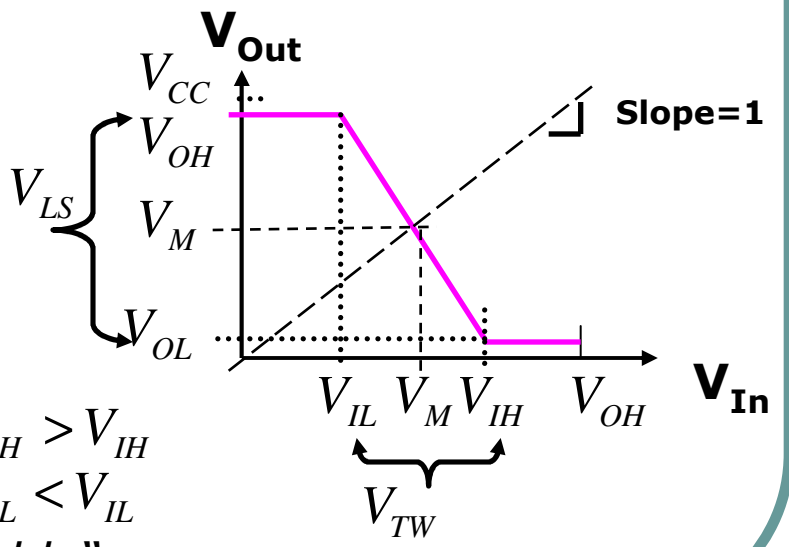
Voltage Transfer Characteristics (VTC) of Inverters

- Ideal



- Practical

1. V_{OH}: Output high voltage level
2. V_{OL}: Output low voltage level
3. V_{IL}: Max. Input voltage that provides high output voltage
4. V_{IH}: Min. Input voltage that provides low output voltage
5. V_M: Midpoint (V_{Out}=V_{In})ideally~=Vcc/2
6. V_{LS}: Logic swing voltage. change in input to cause a change in output
5. V_{TW}: Transition width



The outputs of present inverter will be inputs to the next gate,

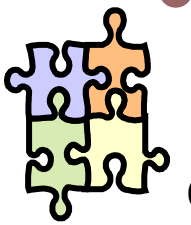
$V_{OH} > V_{IH}$

$V_{OL} < V_{IL}$

"Low and High levels must be distinguishable"

Voltage Transfer Characteristics (VTC) of Inverters

- Example



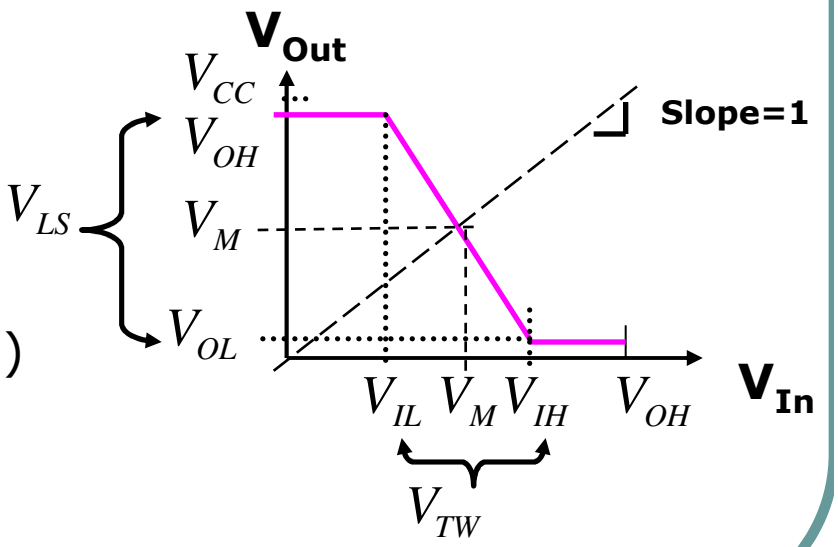
Assume V_{OH}= 4.3 V, V_{OL}= 0.2 V, V_{IL}= 0.7 V, V_{IH}= 0.9 V

Calculate V_{LS}, V_{TW}, and V_M

- Solution

V_{LS}= 4.1 V,
V_{TW}= 0.2 V,

Y-y0=slope(x-x0)
Y-4.3=[(0.2-4.3)/(0.9-0.7)](x-0.7)
Y==x → y=0.867 V
→ V_M= 0.867 V far from Vcc/2



Noise in Digital Ccts.

- Noise: Fluctuations (variations, degredations) of the steady state voltage levels
- Noise margins:
  - Low noise margin
  - High noise margin

$$V_{NML} = V_{IL} - V_{OL}$$

$$V_{NMH} = V_{OH} - V_{IH}$$

Safety margins (have to be positive)

- Noise Sensitivities:
  - Low noise sensitivity
  - High noise sensitivity

$$V_{NSL} = V_M - V_{OL}$$

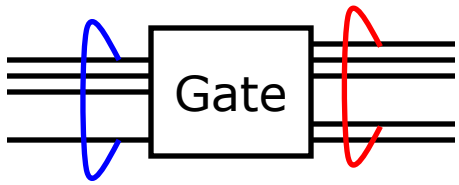
$$V_{NSH} = V_{OH} - V_M$$

- Noise Immunities (ability of a gate to reject noise)
  - Low noise immunity

$$V_{NIL} = V_{NSL} / V_{LS}$$

$$V_{NIH} = V_{NSH} / V_{LS}$$

Fan-In and Fan-Out



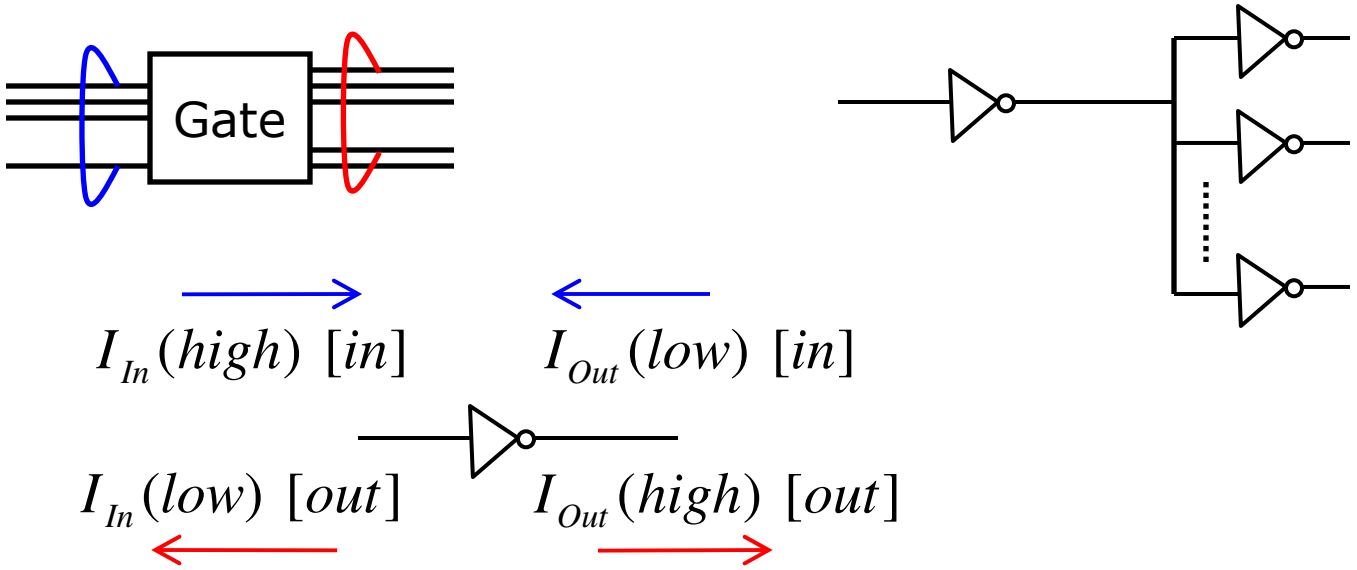
- Fan-In: (less concern)

  Number of inputs of a gate.

- Fan-Out:

  Number of outputs of a gate.

Maximum Fan-Out of a Digital Gate

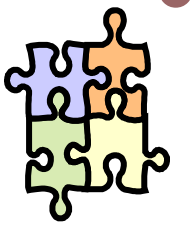


- Maximum Fan-out=min{N_{low}, N_{high}}

$$N_{low} = \frac{I_{Out}(low)}{I_{In}(low)} \qquad N_{high} = \frac{I_{Out}(high)}{I_{In}(high)}$$

Maximum Fan-Out of a Digital Gate

- Example

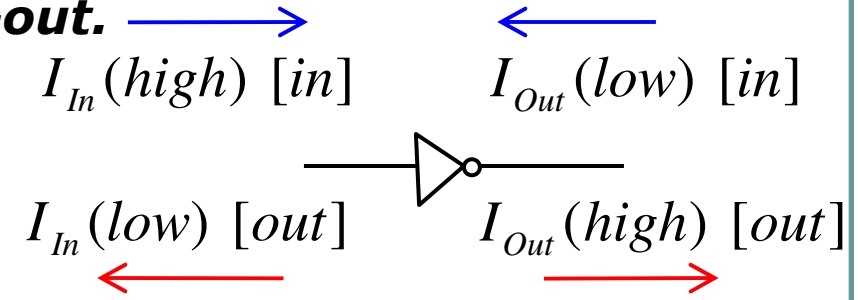


Assume $I_{In}(high) = 98.9\mu A$ $I_{In}(low) = 2.43mA$

$I_{Out}(high) = 71.4mA$ $I_{Out}(low) = 54.3mA$

Calculate *the maximum fan-out.*

- Solution



$$N_{low} = \frac{I_{Out}(low)}{I_{In}(low)} = \frac{54.3}{2.43} = 22.3$$

$$N_{high} = \frac{I_{Out}(high)}{I_{In}(high)} = \frac{71.4}{0.0989} = 721.9$$

⇨ ***maximum fan-out= 22***

Rounded to the nearest lowest integer

Transient Characteristics

- Switching speed

Associated with charging and discharging the load capacitances

Ch

t_d = delay time

t_r = rise time

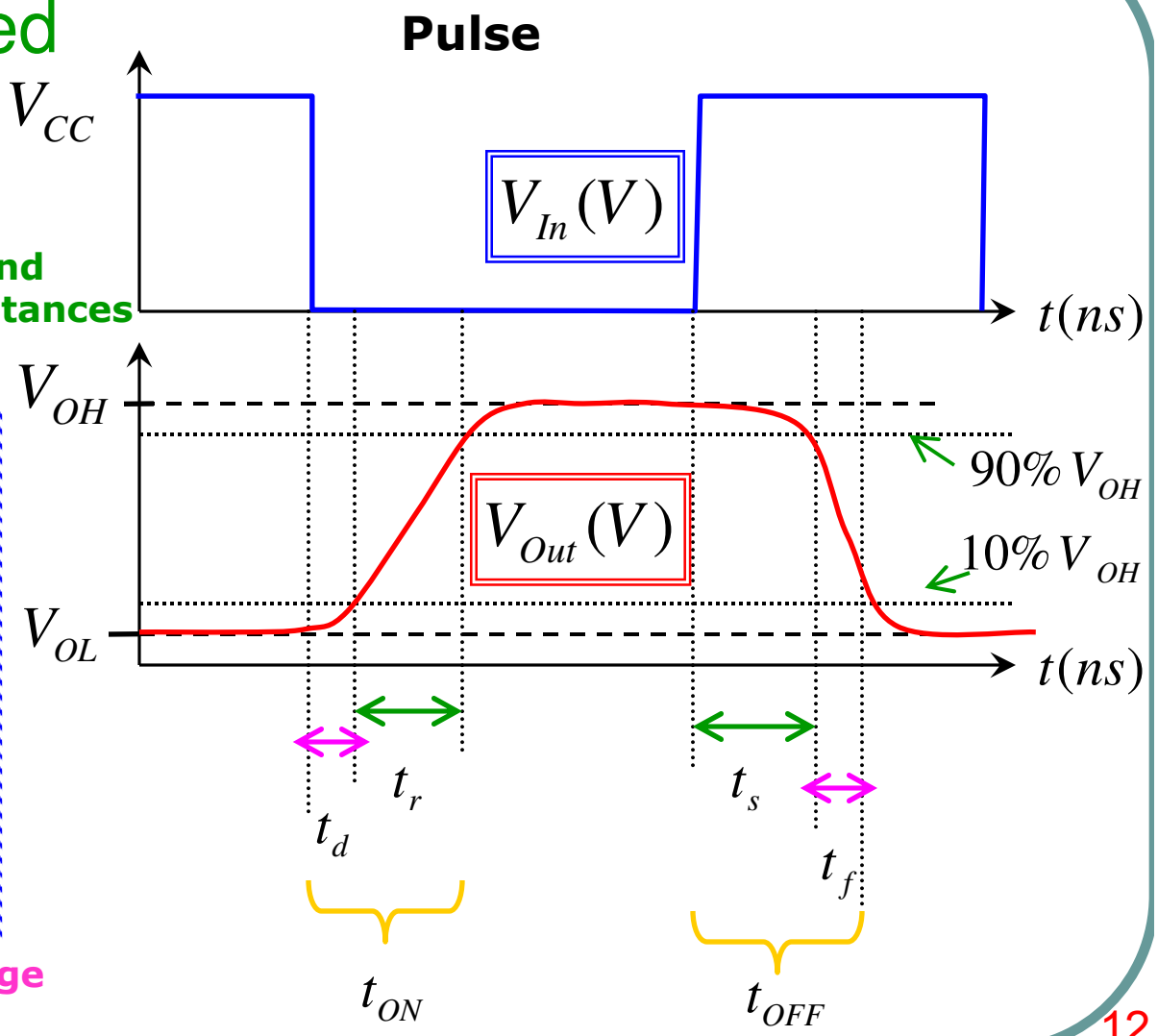
t_s = storage time

t_f = fall time

t_{ON} = turn - on time = $t_d + t_r$

t_{OFF} = turn - off time = $t_s + t_f$

Associated with stored charge of pn junction



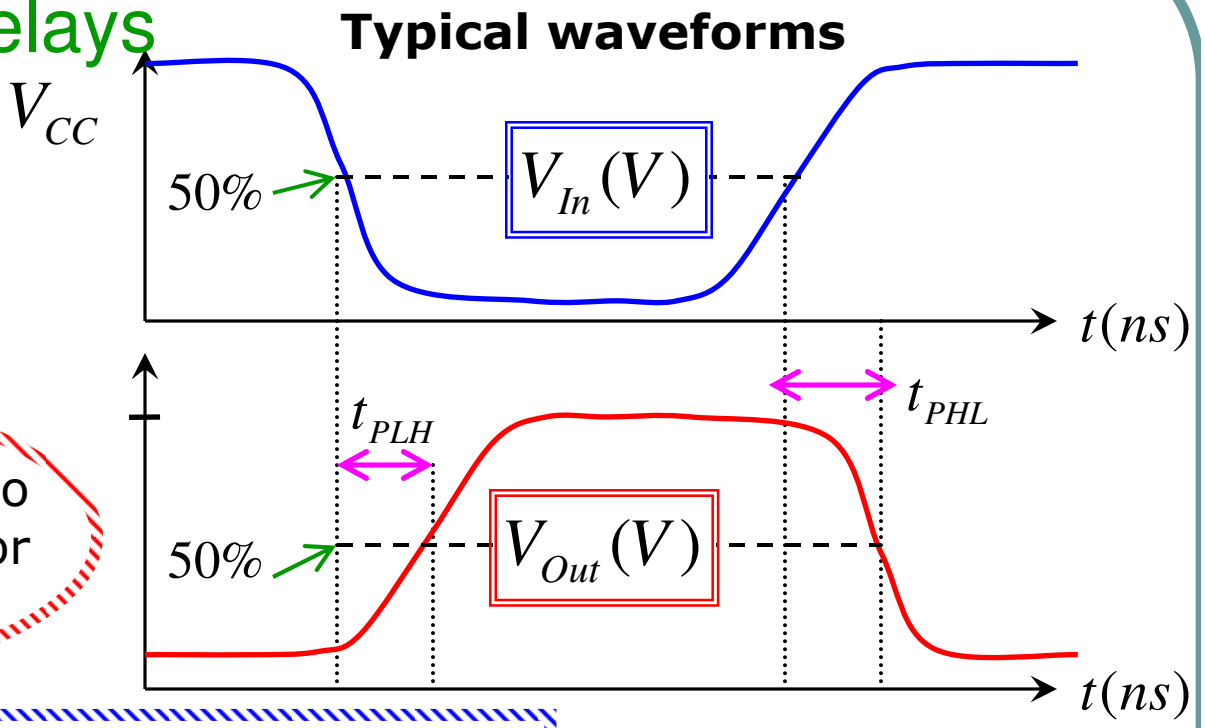
Transient Characteristics

- Switching voltage high ⇨ low requires a finite amount of time, i.e., the output does not respond immediately (delay).
- *Propagation delay time (PDT)*: is the time interval btween the application of an input and the response of the resulting output.
- In BJTs, PDT is caused by the time required to store and remove the charge from the base region.
- In MOSFETs, PDT is caused by the metal oxide capacitance

Transient Characteristics

Ch 1

- Propagation delays



The 50% points are used to define the time required for the output to respond

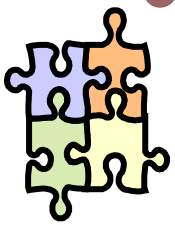
t_{PLH} = refers to low - to - high transition of the output

t_{PHL} = refers to high - to - low transition of the output

$$t_p(avg) = \frac{t_{PLH} + t_{PHL}}{2}$$

Transient Characteristics

- Example

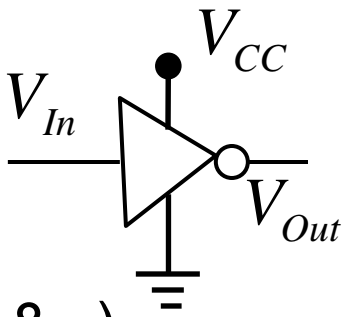


See example **1.5** on page 9

Transient Characteristics

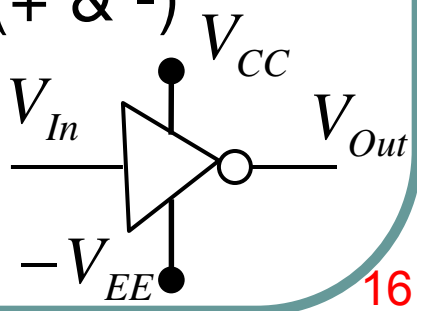
- Power dissipation:
  - An ideal gate has a single power supply
  - The power dissipated equals the power supplied
  - The dissipated power in logic high and logic low states may differ

$$P_{CC}(avg) = \frac{P_{CC}(OH) + P_{CC}(OL)}{2} = \left(\frac{I_{CC}(OH) + I_{CC}(OL)}{2}\right) V_{CC}$$



  - Some gates have two power supplies (+ & -)

$$P_{DISS}(avg) = P_{CC}(avg) + P_{EE}(avg) = \left(\frac{I_{CC}(OH) + I_{CC}(OL)}{2}\right) V_{CC} + \left(\frac{I_{EE}(OH) + I_{EE}(OL)}{2}\right) V_{EE}$$



Transient Characteristics

- Power-Delay product (*speed-power product*):
  - Low power dissipation and short propagation delay are desirable for digital ICs.
  - But, faster propagation delay times are achieved at the cost of increased power dissipation.
  - As a figure of merit,power-delay product is defined as

$$PD = P_{DISS}(avg) \times t_p(avg) \quad [J]: joules$$

  - The smaller the PD is, the more ideal the gate is. *Ideally PD=0 J*.

End

Assignment # 1

- HW #1:Solve Problems: 1.1, 1.5, 1.12, 1.22, and 1.24